WHAT IS CLAIMED IS:

1. A program storage device readable by a computer, the program storage device tangibly embodying one or more programs of instructions executable by the computer to perform operations for determining when to perform an error recovery instruction, the operations comprising:

receiving an error recovery instruction;

beginning a timeout task;

monitoring processor status to determine a time to perform the error recovery instruction; and

performing the error recovery instruction when the monitoring determines a time for performing the error recovery.

2. The program storage device of claim 1 further comprising forcing an execution of the error recovery instruction when the timeout task expires before the monitoring determines a time to perform the error recovery instruction.

3. The program storage device of claim 2 further comprising resuming normal operations after performing the error recovery instruction.

4. The program storage device of claim 1, wherein the monitoring processor status to determine a time to perform the error recovery instruction further comprises:

monitoring a processor interface for an idle condition;

withholding access to the processor interface when the idle condition is detected;

after access to the processor interface is withheld, interrogating all data transfer paths to determine when all the data paths are idle; and

identifying the time to perform the error recovery instruction when all data transfer paths are idle.

5. The program storage device of claim 4 further comprising resuming normal operations after performing the error recovery instruction.

6. The program storage device of claim 1 further comprising resuming normal operations after performing the error recovery instruction.

7. A program storage device readable by a computer, the program storage device tangibly embodying one or more programs of instructions executable by the computer to perform operations for determining when to perform an error recovery instruction, the operations comprising:

receiving an error recovery instruction;

monitoring processor status to determine a time to perform the error recovery instruction; and

performing the error recovery instruction when the monitoring determines a time for performing the error recovery.

8. The program storage device of claim 7 further comprising beginning a timeout task after receiving the error recovery instruction and forcing an execution of the error recovery instruction when the timeout task expires before the monitoring determines a time to perform the error recovery instruction.

9. The program storage device of claim 8 further comprising resuming normal operations after performing the error recovery instruction.

10. The program storage device of claim 7, wherein the monitoring processor status to determine a time to perform the error recovery instruction further comprises:

monitoring a processor interface for an idle condition;

withholding access to the processor interface when the idle condition is detected;

after access to the processor interface is withheld, interrogating all data transfer paths to determine when all the data paths are idle; and

identifying the time to perform the error recovery instruction when all data transfer paths are idle.

11. The program storage device of claim 10 further comprising resuming normal operations after performing the error recovery instruction.

12. The program storage device of claim 7 further comprising resuming normal operations after performing the error recovery instruction.

13. An apparatus for quiescing processor control logic upon receipt of an error recovery instruction, comprising:

self-quiesce logic, coupled to the timer, the self-quiesce logic receiving an error recovery instruction; and

a timer for determining when to force execution of the error recovery instruction;

wherein the self-quiesce logic initiates the timer when the error recovery instruction is received, begins to monitor processor status to determine a time to perform the error recovery instruction and performs the error recovery instruction when the monitoring determines a time for performing the error recovery.

14. The apparatus of claim 13, wherein the self-quiesce logic forces an execution of the error recovery instruction when the timer expires before the self-quiesce logic determines a time to perform the error recovery instruction.

15. The apparatus of claim 14, wherein the self-quiesce logic allows resuming normal operations after the error recovery instruction is performed.

16. The apparatus of claim 13, wherein the self-quiesce logic monitors processor status to determine a time to perform the error recovery instruction by monitoring a processor interface for an idle condition, withholding access to the processor interface when the idle condition is detected, after access to the processor interface is withheld, interrogating all data transfer paths to determine when all the data paths are idle and identifying the time to perform the error recovery instruction when all data transfer paths are idle.

17. The apparatus of claim 16, wherein the self-quiesce logic allows resuming normal operations after the error recovery instruction is performed.

18. The apparatus of claim 13, wherein the self-quiesce logic allows resuming normal operations after the error recovery instruction is performed.

19. An apparatus for quiescing processor control logic upon receipt of an error recovery instruction, comprising:

a processor for executing instructions; and

self-quiesce logic, coupled to the processor, the self-quiesce logic detecting an error recovery instruction, wherein the self-quiesce logic monitors processor status to determine a time to perform the error recovery instruction and performs the error recovery instruction when the monitoring determines a time for performing the error recovery.

20. The apparatus of claim 19 further comprising a timer for determining when to abort the monitoring of processor status and data path activity and cause an execution of the error recovery instruction.

21. The apparatus of claim 20, wherein the self-quiesce logic causes normal operations to be resumed after performing the error recovery instruction.

22. The apparatus of claim 19, wherein the self-quiesce logic monitors processor status to determine a time to perform the error recovery instruction by monitoring a processor interface for an idle condition, withholding access to the processor interface when the idle condition is detected, after access to the processor interface is withheld, interrogating all data transfer paths to determine when all the data paths are idle and identifying the time to perform the error recovery instruction when all data transfer paths are idle.

23. The apparatus of claim 22, wherein the self-quiesce logic causes normal operations to be resumed after performing the error recovery instruction.

24. The apparatus of claim 19, wherein the self-quiesce logic causes normal operations to be resumed after performing the error recovery instruction.

25. A method for determining when to perform an error recovery instruction, comprising:

receiving an error recovery instruction;

beginning a timeout task;

monitoring processor status to determine a time to perform the error recovery instruction; and

performing the error recovery instruction when the monitoring determines a time for performing the error recovery.

26. A method for determining when to perform an error recovery instruction, comprising:

receiving an error recovery instruction;

monitoring processor status to determine a time to perform the error recovery instruction; and

performing the error recovery instruction when the monitoring determines a time for performing the error recovery.

27. An apparatus for quiescing processor control logic upon receipt of an error recovery instruction, comprising:

means for receiving an error recovery instruction; and

means for determining when to force execution of the error recovery instruction;

wherein the means for receiving the error recovery instruction initiates the timer when the error recovery instruction is received, begins to monitor processor status to determine a time to perform the error recovery instruction and performs the error recovery instruction when a time for performing the error recovery is determined.

28. An apparatus for quiescing processor control logic upon receipt of an error recovery instruction, comprising:

means for executing instructions; and

means, coupled to the means for executing instructions, for detecting an error recovery instruction, monitoring processor status to determine a time to perform the error recovery instruction and performing the error recovery instruction when a time for performing the error recovery is determined.